GEn01 Data Acquisition & Electronics

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Chapter 1

Electronics

1.1 Electronics Strategy

The electronics will be the same as in 1998 but with the following improvements:

- The neutron detector electronics will have its own FASTBUS (ADC and TDC) and VME (scaler) crate. Minimal cannibalization of the SOS electronics therefore. Also CAMAC and NIM electronics for a generic third arm is available for 200 channels.
- In 1998 electronics dead-time was introduced into the system due to the high rate line (OR of all neutron detector bars) that was used to form the coincidence with the electron. To avoid electronics dead-time the following measures are planned:
    1. Data taking with "Open Trigger": The neutron detector is read out for each electron trigger. Coincidences are formed in analysis. This requires the data acquisition to run in "buffered" mode due to the event rate ($\simeq$900 Hz for 100 nA at $Q^2 = 0.5$). "Buffered" mode is nowadays standard.
    2. Coincidence between 14 subsets of the neutron detector and the elecron trigger serves as a coincidence trigger. This is only a backup in case the data acquisition is not able to run "buffered" for some reason.
    3. Measurement of the electronics deadtime using a pulser system, which was available at the end of the 1998 run but not in use yet. The only documentation on this is an elog entry from October 27, 1998 (entry number: 9692)

1.1.1 Coincidence

The plan is to make a coincidence between 14 subsets (OR outputs of the L4516) of the neutron detector (NDET) and the HMS electron trigger (output of EL-

REAL). See figures 1.1, 1.2 and 1.3. This could be accomplished with commercially available modules, but it would require several steps and modules (multiplication of electron trigger, coincidence, making the OR of all outputs), which becomes a space and timing issue:
Forming the coincidence at the location of the NDET electronics requires to send the electron trigger over to the NDET racks and the coincidence output back to the trigger electronics, which uses up too much of the available time bandwidth. Therefore the coincidence needs to made at the location of the HMS electronics, but there is only a limited number of slots in the HMS crates available.
The solution is a single coincidence module (NIM) which is custom built by the electronics group at Jlab. It accepts 16 inputs (NDET subsets) which can be gated by a single input (electron trigger). It has individual outputs of fixed length (30ns) and one OR output (variable length). Upon overlap of gate and one or more of the 16 inputs the corresponding individual outputs as well as the OR will fire. The individual outputs will be sent to scalers while the OR output serves as coincidence trigger. The timing of the outputs is determined by the leading edge of the later signal in the overlap. It can therefore be either electron or NDET. If electron time is desired for the trigger another coincidence needs to be made between the OR (wide) and the delayed electron (narrow and centered in the OR). The module will be located in one of the HMS NIM bins.

1.1.2 Timing

Ideally the HMS and NDET signal arrive simultaniously at the coincidence module. However the total delays of both arms are only fixed/known within certain limits. The approach is to time the electronics such that an early electron does not have to wait for a late neutron. This is motivated by the fact that the HMS electronics does not have that much delay time to spare and therefore any additional delay should be on the NDET side.
An early NDET signal still arrives only 8 ns before the electron at the splitter, because the processing of the signals in the NDET logic (84 ns) needs considerably less time than in the HMS logic (127 ns). Therefore there is no danger that the NDET runs out of time while waiting for the electron. The actual delays are specified in section 1.2.

1.2 Calculation of Delays

We need to specify the length of the cables for the neutron detector. For that all the delays from the target in the hall to the logic circuit upstairs in the counting house have to be taken into account. The table below summarizes the numbers.

HMS	Delay	Σ	NDET	Delay 2"/5" PM	Σ 2"/5" PM
TOF (S1)	80	80	TOF	20±10	20
TT scin	5±2	85	TT scin	8±3	28
TT PM	20±2	105	TT PM	36/68±2	64/96
PM-PPhut	50	155	PM-AMP	54	118/150
			AMP	3	121/153
			AMP-PP1	150/118	271
PPhut-PPH	240±1	395	PP1-PP2	122±1	393
PPH-PP3	6	401	PP2-PP3	23	416
PP3-CHPP	250±1	651	PP3-CHPP	250±1	666
CHPP-S	12	663	CHPP-S	12	678
S-COIN	127	790±6	S-COIN	89	767±17

HMS notes:

TOF (S1): This is the electron Time of Flight from the target to the first hodoscope. The TOF to S2 is 8 ns longer. In the hodoscope electronics are adjustable delay boxes which compensate for that difference, i.e. S1, S1X and S1Y are delayed with respect to S2, S2x and S2Y by 8 ns (see figure 1.4). Since the delay times through the whole HMS electronics were measured with a S1 signal (see S-COIN) we use the TOF to S1 here.
TT scin: Transit time in scintillators (from Petitjean/ McFarlane calculation in 1998).
TT PM: photomultiplier transit time according to specifications.
PM ... S: Leading the signals from the PM output through various patch panels to the splitter upstairs (Numbers from Bill Vulcan).
S-COIN: The delay from the Splitter output through the whole HMS logic to the input of the custom built coincidence unit. The delay time from the Splitter to the output of ELREAL was measured 12/14/00 using a pulser which was fed into H1X1+ and H1X1-. ELHI was set to 1/3 and SCIN was set to 1/4. The measured value was 122 ns. 5 ns are added for the connection to COIN

NDET notes:

NDET TOF: The variation is due to different kinematics and TOF distances.
TT scin: Transit time in scintillators (from Petitjean/ McFarlane calculation in 1998).
TT PM: The transit time of photomultipliers depends on PM type and operating HV. The neutron detector uses 2 types of photomultipliers (2" and 5" diameter) which are operated below nominal HV. The numbers are from Glen Warren who did tests for this particuar conditions.

PM-AMP: cable from PM output to amplifier.
AMP: amplifier input/output delay
AMP-PP1: cable from amplifier to first patch panel on the wall. This is where the different PM TTs are compensated and the neutron detector is timed with respect to the electron as discussed in section 1.1.2.
PP1 .. S: Leading the signals through various patch panels to the splitters upstairs (Numbers from Bill Vulcan).
S-COIN: The delay from the Splitter output through the NDET logic to the input of the custom built coincidence unit. The signals need to be transported from the splitter to the NDET electronics first (32 ns) and finally to the HMS electronics (another 32 ns), where the COIN unit is. The delays inbetweene are calculated from input/output delay specifications of the electronics modules and from assumed cable lengths.

1.3 Cable List

There are 180 unused channels available that connect the hall patch panel with the counting house patch panel. We plan on 300 channels and therefore we will have to use 120 SOS channels.

For the 120 SOS cables we will use the existing SOS transition boxes with the existing delays attached to them. The SOS signals will be disconnected at the CHPP and at the transition box inputs/outputs (50 Ohm coax ribbon cable).

The other 180 channels will be equipped in the same way as HMS and SOS are. They can be considered as a permanent third arm installation. They will need new splitter boxes, transition boxes and delays, which will be located right next to the existing SOS and HMS ones. One potential problem is enough space for the additional 180 delay bundles. This will be looked at during setup time.

The following table lists the cables that are needed. **The length of the cable is quoted in nanoseconds, which is the crucial quantity and by which the cables should be ordered**. For the RG58 cable also the length in feet is given, which is calculated from the signal propagation velocity (0.75 ft/ns for the RG58A/U according to Joe Beaufait, 0.84 ft/ns for the RG213 according to Bill Vulcan). A quantity of 300+10 means that 300 are actually needed and 10 is the suggested number of spares.

Qty	Type	Length	Usage
300+10	BNC-RG58-Lemo	54 ns (40.5 ft)	1)
112+5	BNC-RG58-Lemo	118 ns (88.5 ft)	2)
188+5	BNC-RG58-Lemo	150 ns (112.5 ft)	3)
300	BNC-RG213-BNC	23 ns (19.3 ft)	4)
180+5	BNC-RG58-BNC	390 ns (292.5 ft)	5)
300+5	BNC-RG188-Lemo	12 ns	6)
15+5	34 pin Shielded 50 Ohm	≥16 ft	7)
25+5	34 pin Shielded 50 Ohm	≥26 ft	8)
300+15	Lemo-RG188-Lemo	32 ns	10)
20	Lemo-RG188-Lemo	32 ns	11)
20	Lemo-RG188-Lemo	32 ns	12)
20	Lemo-RG188-Lemo	32ns	13)
25	Lemo-RG188-Lemo	32ns	14)
100	Lemo-RG188-Lemo	16 ns	14)
100	Lemo-RG188-Lemo	8 ns	14)
100	Lemo-RG188-Lemo	4 ns	14)
100	Lemo-RG188-Lemo	2 ns	14)
100	Lemo-RG188-Lemo	1 ns	14)
300	HV cables	100 ft	15)

Usage:

1) Connects photomultiplier outputs with amplifier inputs
2) Connects amplifier outputs of the 5" PMs with first patch panel on the wall (PP1).
3) same as 2) but for the 2" PMs.
4) Jumper cables from 2^{nd} wall patch panel (PP2) to hall patch panel (PP3).
5) Delay cable for analog signals (ADC). Connected to Transition Boxes as Bundles. Only needed for the 180 third arm channels.
6) Connects counting house patch panel (CHPP) with splitter.
7) Connects splitter output (50 Ohm ECL) with transition box inputs. Only needed for the 180 third arm channels.
8) Connects transition box outputs with ADC inputs (analog signals)
10) Connects splitter with Discriminator (L4413) in NDET electronics
11) Connects L4516 outputs (NDET electronics) with custom built coincidence module (in HMS electronics)
12) Connects custom built coincidence outputs with scalers in NDET electronics.
13) Connects various outputs of NDET electronics to patch panel that leads to visual scalers
14) general purpose for NDET logic
15) HV supply for PMs

Related material that is needed:

-) A few rolls of 17 pair Vari Twist Cable and 34 pin connectors
-) 2 pin twisted pair cables of various lengths
-)5 passive splitter boxes (UVA type): 4×16 channel each
-)10 Transition Boxes: 2×16 channel each
-) Lemo and BNC converters, barrels etc.

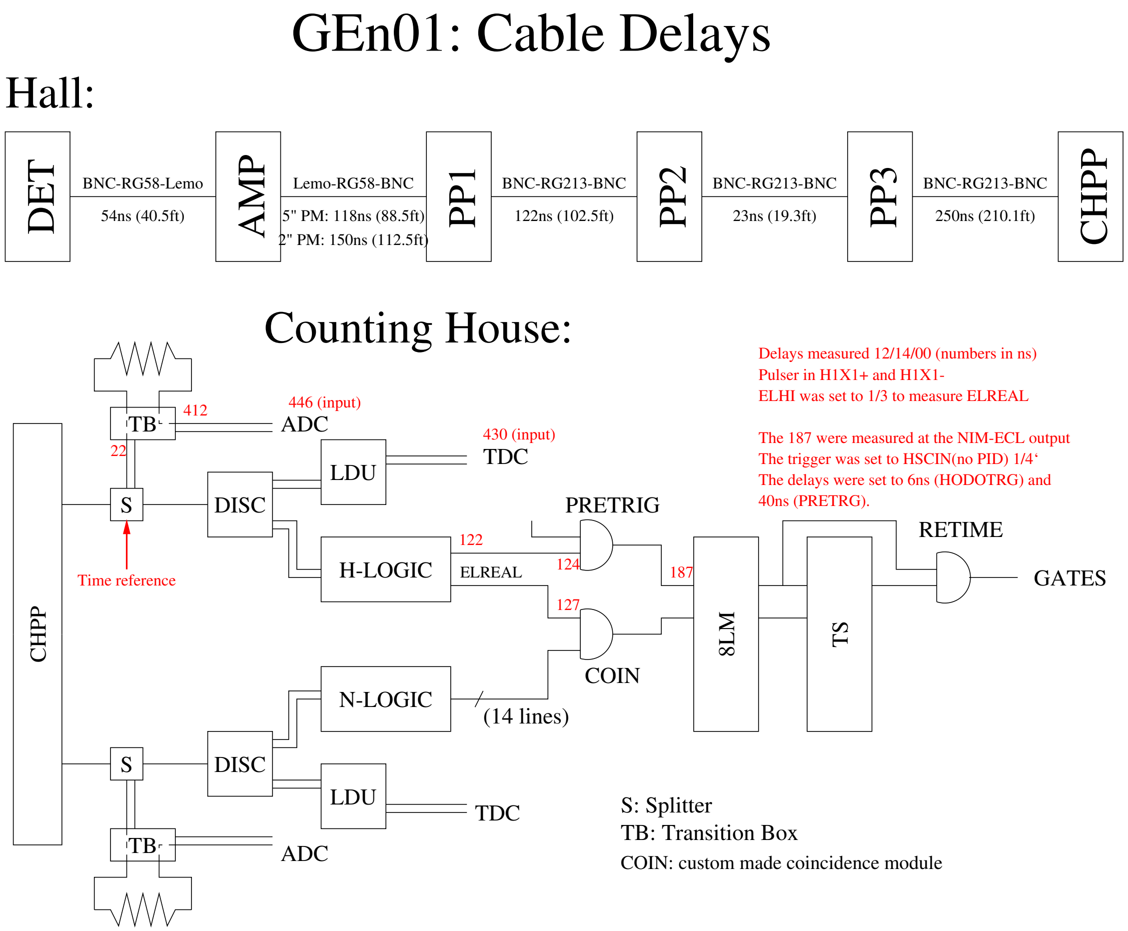


Figure 1.1: Schematic of signal path from detector to counting house patch panel (CHPP). Schematic layout of the electronics in the counting house with measured delays.

1.4 NDET Logic

The neutron detector electronics is the same as in 98, except that we are avoiding the discriminators after the L4516 and go directly to the coincidence module. Also the outputs of the paddles are not fed to the 8LM anymore. All the Logic delay Units (LDU) used in this run are Basel modules. For details see figure 1.2.

1.5 HMS Logic

We are using the standard Hall C HMS electronics, which does not require any further setup except timing adjustments. For details see figures 1.3 and 1.4.

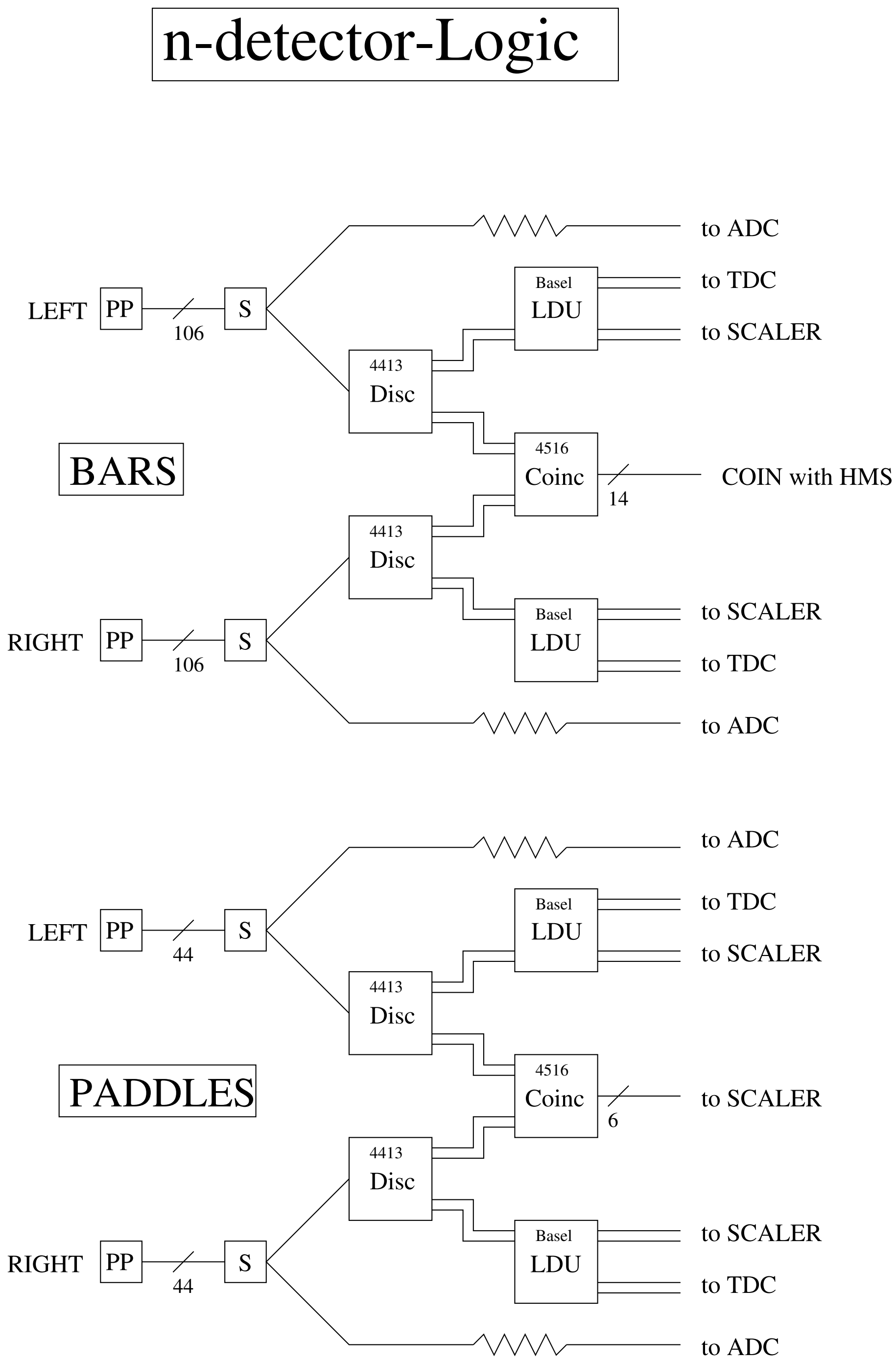


Figure 1.2: Schematic layout of the NDET logic

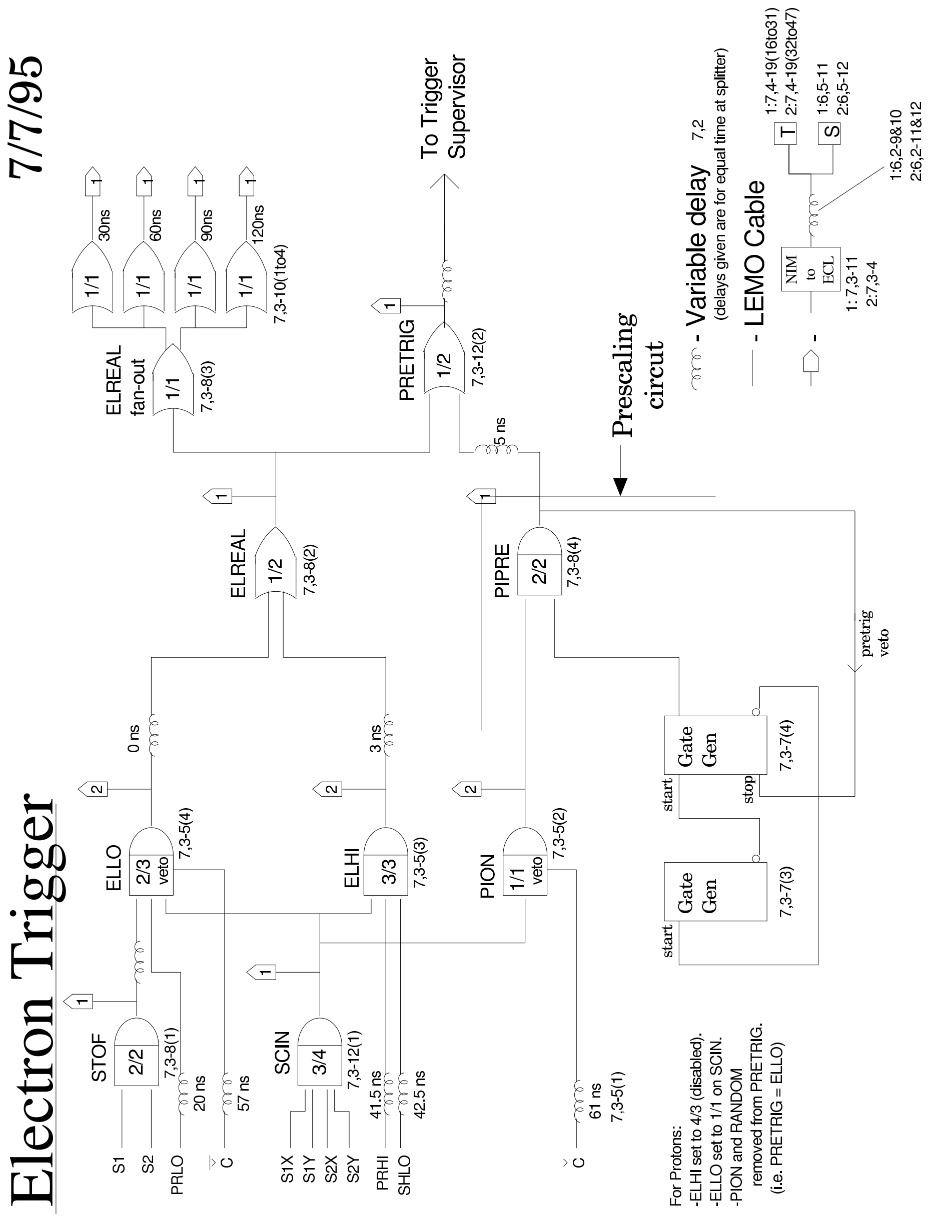


Figure 1.3: HMS trigger

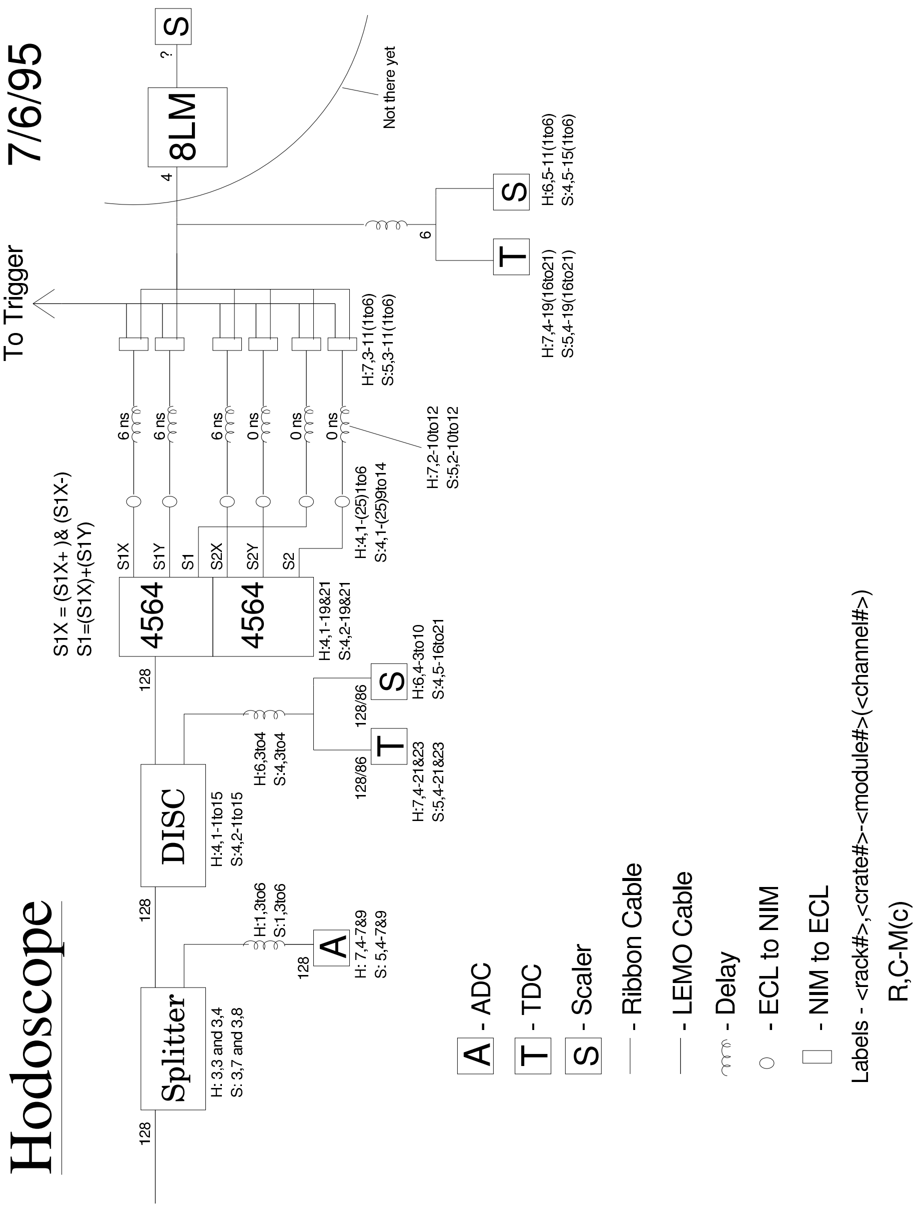


Figure 1.4: HMS hodoscope electronics

1.6 Trigger Logic

The philosophy is to leave the standard HMS-SOS system untouched. Signals for the neutron detector are just added and all changes are accomplished in software as far as possible.

Heart of the trigger system are the Octal Logic Matrix (8LM), the Trigger Supervisor (TS) and the retiming circuits. The basic setup is visualized in figure 1.5.

We are using two 8LMs as in 1998, but we are forming the coincidence between the HMS and the NDET in the custom built coincidence module (see section 1.1.1) and not in the 8LM as in 1998. Cabling and programming of the 8LMs is specified in tables 1.1, 1.2 and 1.3.

The TS Inputs are listed in table 2.2. The scaler trigger is not fed into an ordinary trigger input as done previously. We are using a new TS, which has a "Programmable Event" feature that should make scaler readout more reliable (see section 2.3.1).

Timing of the ADC and TDC gates will be determined by the HMS time for both HMS and NDET.

Table 1.1: 8LM Inputs (for both 8LMs). HMS and SOS are the PRETRIG signals from the HMS and SOS circuits. Ped is the Pedestal pulser. TS GO indicates an active DAQ. TS EN1 indicates that physics trigger are enabled (after Pedestals are taken). TS BUSY indicates that DAQ is busy processing trigger and does not accept any other trigger. These are all outputs of the Trigger Supervisor (TS). e$\star$B is the output of the custom built coincidence module. Cosmics is the output of the NDET cosmics trigger circuit. Laser is the output from the pin diode. Scaler is the signal that triggers the readout of the helicity gated scalers during PHT. PHT is the "Period of Helicity Transition", during which the electronics is blanked. The last two signals are part of the "Howard Fenker" helicity circuit (see sections 1.7 and 1.8).

8LM Inputs	Signal
I0	HMS
I1	SOS
I2	PED
I3	TS GO
I4	TS EN1
I5	TS BUSY
I6	e$\star$B
I7	COSMICS
I8	LASER
I9	SCALER
I10	PHT

Table 1.2: Outputs for first 8LM: same as standard HMS/SOS running. The SOS related signals can stay low.

8LM output	Signal
Q0	HMS-pretrig = HMS&EN1&(!PHT)
Q1	SOS-pretrig = SOS&EN1&(!PHT)
Q2	COIN-pretrig = HMS&SOS&EN1&(!PHT)
Q3	PED-pretrig = Ped&GO&(!EN1)
Q4	HMS-trig = HMS&EN1&(!PHT)&(!BUSY)
Q5	SOS-trig = SOS&EN1&(!PHT)&(!BUSY)
Q6	COIN-trig = HMS&SOS&EN1&(!PHT)&(!BUSY)
Q7	PED-trig = Ped&GO&(!EN1)&(!BUSY)

Table 1.3: Outputs for second 8LM

8LM output	Signal
Q0	e⋆B-pretrig = e⋆B&EN1&(!PHT)
Q1	LASER-pretrig = LASER&EN1&(!PHT)
Q2	COSMICS-pretrig = COSMICS&EN1&(!PHT)
Q3	e⋆B-trig = e⋆B&EN1&(!PHT)&(!BUSY)
Q4	LASER-trig = LASER&EN1&(!PHT)&(!BUSY)
Q5	COSMICS-trig = COSMICS&EN1&(!PHT)&(!BUSY)
Q6	SCALER-trig = SCALER&EN1&(PHT)
Q7	-

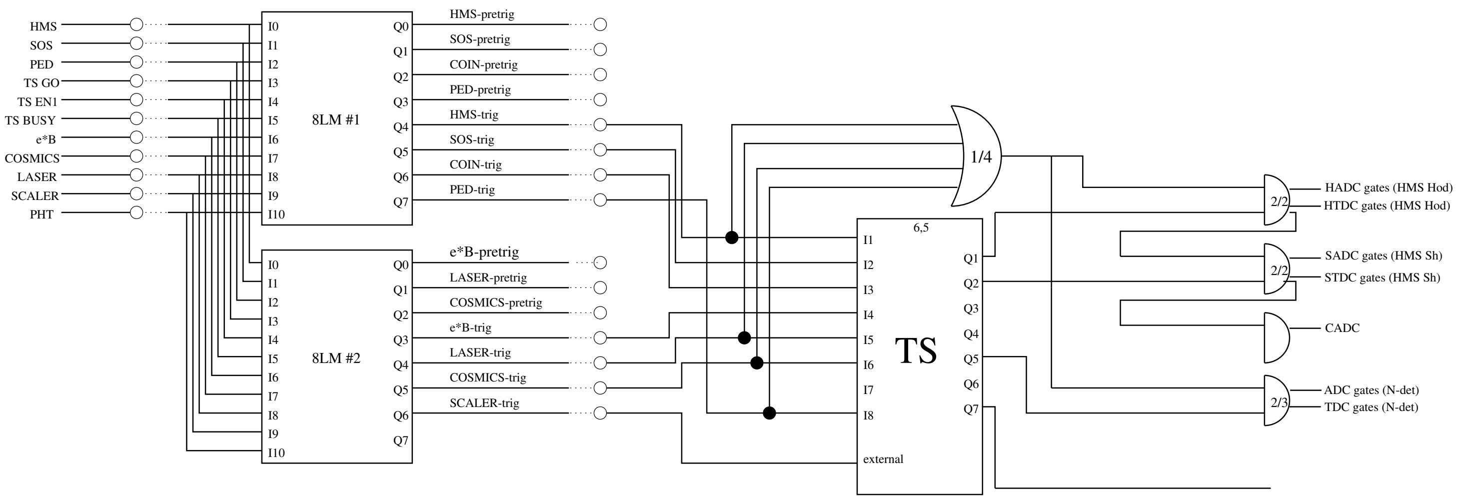


Figure 1.5: Basic trigger setup

1.7 Helicity

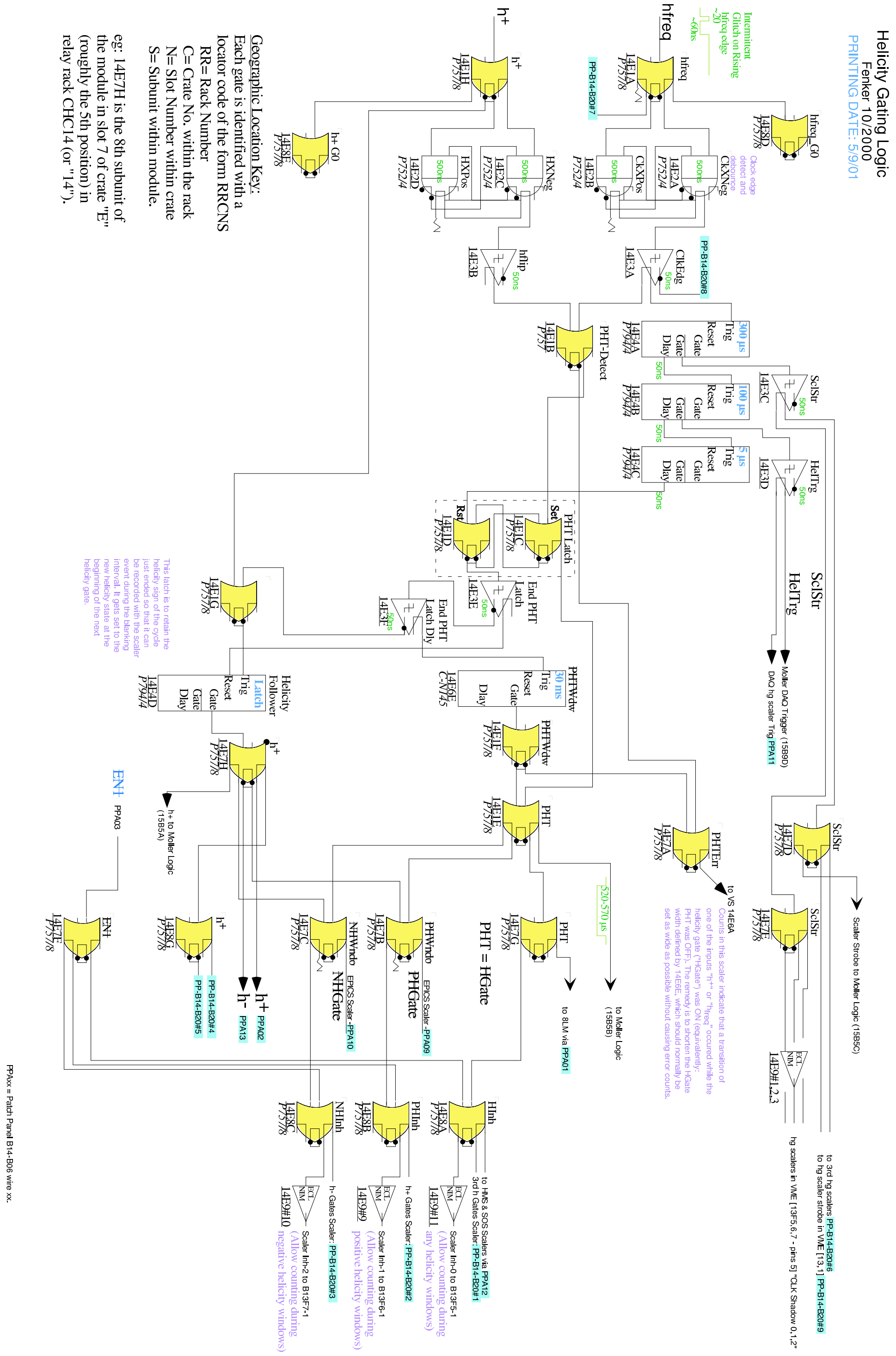
The helicity is changing in a pairwise pseudorandom mode with a frequency of 30 Hz.

We are using the helicity circuit established and maintained by Howard Fenker for the E93-038 experiment (see figure 1.6).

This circuit provides the following signals of importance:

- h+: Level that indicates positive helicity when high.
- h-: Level that indicates negative helicity when high.
- PHT: "Period of Helicity Transition". This is a signal that appears at the moment of potential helicity change. It has an adjustable width of 500-1000 μs, and is used to blank the electronics during this period.
- Scaler-trig (Hel Trg): This signal appears within the PHT, a defined time after the leading edge. It is used to clock the helicity gated scalers (copy scaler value to FIFO) and to trigger the scaler readout of the helicityy gated scalers.
- Scaler-clock (SclStr): This signal appears within the PHT, a defined time after the leading edge but before the Scaler-trig. It is used to copy the current value of the helicity gated scalers into the FIFO or Shadow register.
- Inhibits of the helicity gated scalers (HInh, PHInh, NHInh)

Figure 1.6: Helicity Circuit



1.8 Scalers

Some of the signals used to gate and trigger the scalers are explained in section 1.7.

We are using three types of scalers:

- Asynchronous scalers: Scalers which are readout every two seconds. There is one set of scalers for the HMS and one set for the NDET (384 channels available) . HMS signal inputs are standard. The NDET inputs are defined in table 1.4.
- Helicity gated scalers: One scaler which counts for h+, one which counts for h- and one which counts for both for consistency check. The scalers will be clocked (with Scaler-clock) and read out (with Scaler-trig) during each PHT. Signal inputs are listed in table 1.5.
- Event by Event Scaler: We have one dedicated scaler which is read out for every event. The scaler will be clocked using the OR between OR Level 1 Trigger (TS output) and Scaler-clock. The inputs are listed in table 1.6.

Gating of the scalers is defined in table 1.7.

Table 1.4: Proposed inputs of asynchronous NDET scalers

Channel	Signal
1..320	NDET singles (LDU output)
321..326	PADDLES Coinc (L4516 output)
327..340	e$\star$B(subsets)
341	e$\star$B
342	HMS
343	PED
344	LASER
345	SCALER
346	COSMICS
347	1 MHz Clock
348	BCM 1
349	BCM2
350	Gates NDET

Table 1.5: Proposed inputs of helicity gated scalers. there are 32 channels available. The signals need to be tripled, one for h- scaler, one for h+ scaler and one for h+&h- scaler.

Channel	Signal
1	1 MHz Clock
2	100 MHz Clock
3	BCM 1
4	BCM 2
5	Unser
6	HMS-pretrig
7	HMS-trig
8	e$\star$B-pretrig
9	e$\star$B-trig
10	LASER-pretrig
11	LASER-trig
12	$\overline{TSBUSY}$ & (BCM 1)
13	$\overline{TSBUSY}$ & (100 MHz Clock)
14	(Buffer Full) & (100 MHz Clock)
15	Gates NDET
16	Gates HMS
17	PRETRIG (HMS)
18	ELHI (HMS)
19	ELLO (HMS)

Table 1.6: Proposed inputs of the event by event scaler. There are 32 channels available. Unused channels can be disabled.

Channel	Signal
1	1 MHz clock
2	100 MHz clock
3	BCM 1
4	BCM2

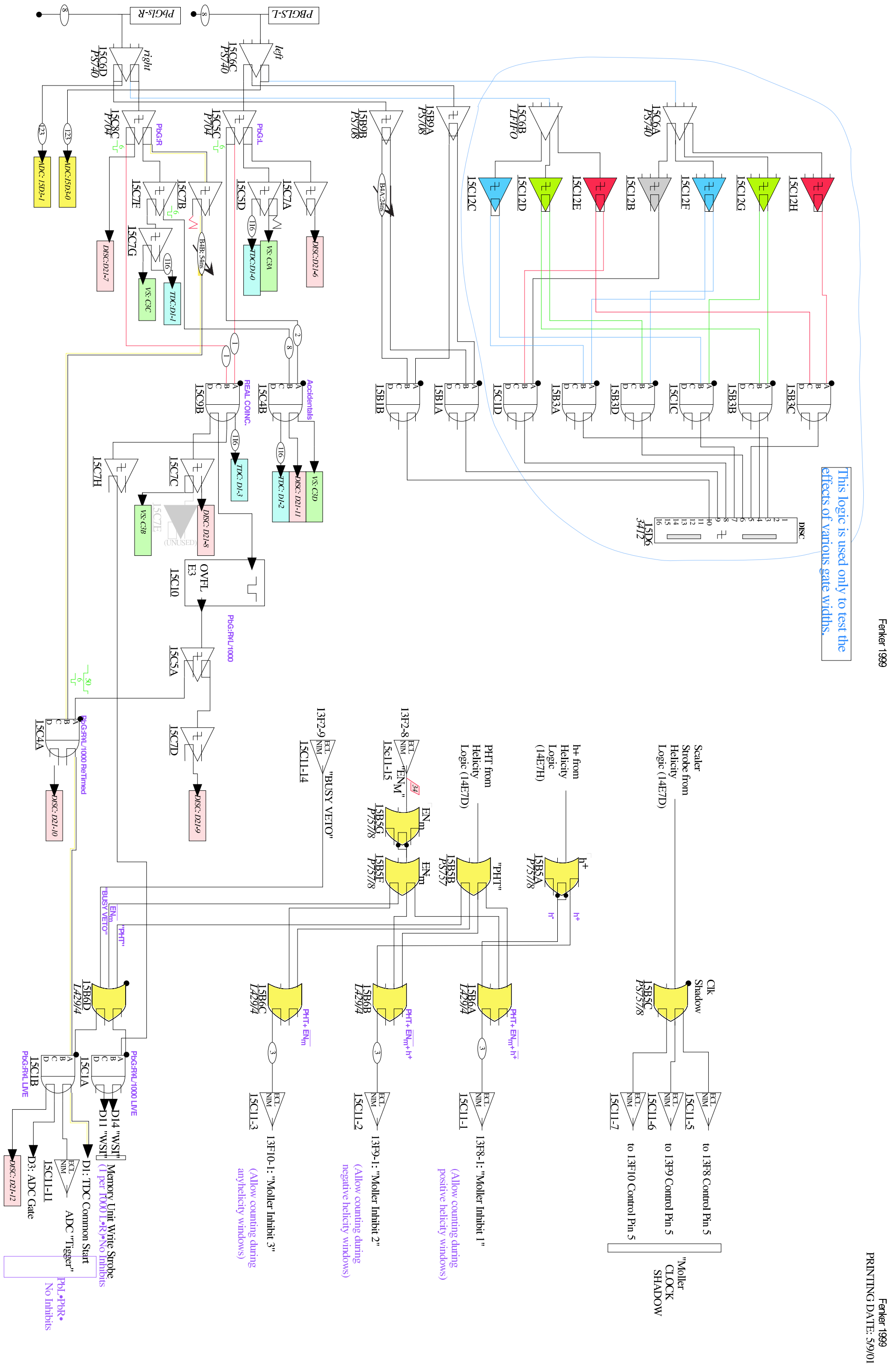
Table 1.7: Gating of the different scaler types

Scaler	Inhibit
Asynchronous	$\overline{TSGO}$+PHT
Helicity gated h+	(h-)+$\overline{EN1}$+PHT
Helicity gated h-	(h+)+$\overline{EN1}$+PHT
Helicity gated h+&h-	$\overline{EN1}$+PHT
Event by Event	$\overline{EN1}$+PHT

1.9 Moller

We are using the standard moller electronics, established and maintained by Howard Fenker. The diagram is shown in figure 1.7.

Figure 1.7: Moller Electronics



Chapter 2

Data Acquisition

2.1 Hardware

Table 2.1 gives an overview over the crates that are used:

Table 2.1: Overview of ADC, TDC and scaler crates

Crate	Type	CPU	Modules	Purpose	Location
1	Fastbus	sfich1	ADC, TDC	HMS hodoscope HMS shower counter HMS cerenkov Raster, SEM	CHC
2	Fastbus	sfihms	TDC	HMS wire chambers	hall C
3	VME	vmec3	Scalers	HMS scalers TS	CHC
4	VME	vmec5	Register	TS Fifo	CHC
5	Fastbus	sfich3	ADC, TDC	NDET signals	CHC
6	VME	vmec9	Scalers	NDET scalers Helicity gated scalers Event by Event scaler	CHC

2.2 Run Types

main: production running type, every crate (1-6) is read out. Switching from Open Trigger to Coincidence trigger is achieved by increasing prescale factor on the HMS-trig.

cosmics: for NDET cosmics running. Only NDET crates (4, 5 and 6) are read out.

hms: Only HMS crates (1, 2 , 3, 4 and 6) are read out

scalers: Only scalers crates (3, 4 and 6) are read out.

2.3 Trigger Supervisor (TS) Programming

The trigger inputs and their status are listed in table 2.2. The signals are defined in the 8LMs (see tables 1.1, 1.2 and 1.3) . The SOS is not needed and therfore are corresponding triggers disabled.

Table 2.2: TS trigger inputs

TS input	Signal	enabled (1)/ disabled(0)			
		main	cosmics	hms	scalers
1	HMS-trig	1	0	1	0
2	SOS-trig	0	0	0	0
3	COIN-trig	0	0	0	0
4	e$\star$B-trig	1	0	0	0
5	LASER-trig	1	1	0	0
6	COSMICS-trig	0	1	0	0
7	-	0	0	0	0
8	PED-trig	1	1	1	0
9	-	0	0	0	0
10	-	0	0	0	0
11	-	0	0	0	0
12	-	0	0	0	0

Event Types and "Level 1 Accept" outputs are dependent on trigger pattern. Details in table 2.3.

2.3.1 "Programmable Events" and Scaler Readout

For the readout of asynchronous and helicity gated scalers we are using the "Programmable Event" feature of the new TS. This event does not get lost even if the TS is busy processing another event. Two of that kind are available. Both can be triggered by software, one via front panel input. Optionally the sync flag can be set. The event type is assigned in a register. No "Level 1 Accepts" are issued.

Helicity Gated Scaler: Readout every PHT. Triggered via front panel input (Scaler trigger from helicity circuit). Event type 5. Synchronization flag asserted.

Asynchronous Scaler: Triggered in software. Readout every 2 seconds. No sync flag. Event type: 10

With this setup we have guaranteed scaler read and synchronization check each helicity flip.

Table 2.3: Programming TS memory: Event types and "Level 1 Accept" outputs are based on trigger input pattern. All patterns are Class 1 Triggers and Level 1 OK. Any trigger pattern not defined here is considered as invalid and an event type 13 is assigned to it with L1 Accept 8 being high.

	Run types										
	main					cosmics			hms		
TS I1 HMS-trig	1	1	0	0/1	-	-	-	-	1	-	-
TS I4 e$\star$B-trig	0	1	1	0/1	-	-	-	-	-	-	-
TS I5 LASER-trig	0	0	0	1	-	0	1	-	-	-	-
TS I6 COSMICS	-	-	-	-	-	1	0/1	-	-	-	-
TS I8 PED-trig	-	-	-	-	1	-	-	1		1	-
Event Type	3	3	3	6	4	7	6	4	1	4	5
L1 Accept 1 HMS	1	1	1	1	1	0	0	0	1	1	0
L1 Accept 2 HMS	1	1	1	1	1	0	0	0	1	1	0
L1 Accept 3 SOS	0	0	0	0	0	0	0	0	0	0	0
L1 Accept 4 SOS	0	0	0	0	0	0	0	0	0	0	0
L1 Accept 5 NDET	1	1	1	1	1	1	1	1	0	0	0
L1 Accept 6 unused	0	0	0	0	0	0	0	0	0	0	0
L1 Accept 7 unused	0	0	0	0	0	0	0	0	0	0	0
L1 Accept 8 any	1	1	1	1	1	1	1	1	1	1	1